Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

Claim 1-2 (Cancelled).

Claim 3. (Currently amended) A computer system comprising:

a host processor;

an attachment bus coupled to the host processor, the attachment bus being inside the computer system, the attachment bus being configured to receive data during time cycles of predetermined length;

a peripheral device coupled to the host processor via the attachment bus, the peripheral device being configured to transfer data from a network to the host processor over the ~~an~~ attachment bus inside the computer system using at least first and second types of data transfers, comprising:

a classifying circuit configured to separate the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer;

a first queue connected to receive the first class of data from the classifying circuit;

a second queue connected to receive the second class of data from the classifying circuit; and

a control circuit configured to place data from the first queue onto the attachment bus at a higher priority than data from the second queue is placed onto the attachment bus;

~~where the bus is configured to receive data during time cycles of predetermined length;~~ where the control

circuit is configured to place at least a minimum amount of data from the first queue onto the attachment bus during each time cycle; where the control circuit is configured to place data from the second queue onto the attachment bus only when the attachment bus is otherwise unoccupied by first class data.

Claim 4. (Previously Presented) The system of claim 3, where the peripheral device includes a network interface component connected to receive the data from a computer network.

Claim 5. (Previously Presented) The system of claim 3, wherein the data includes packetized voice data.

Claim 6. (Currently amended) A computer system comprising:

a host processor;

an attachment bus coupled to the host processor, the attachment bus being inside the computer system;

a peripheral device configured to receive asynchronous transfer mode (ATM) data packets from a network and transfer data to the host processor over the ~~an~~ attachment bus inside the computer system using at least first and second types of data transfers, comprising:

a classifying circuit configured to separate the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer;

a first queue connected to receive the first class of data from the classifying circuit;

a second queue connected to receive the second class of data from the classifying circuit; and

a control circuit configured to place data from the first queue onto the attachment bus at a higher priority than data from the second queue is placed onto the attachment bus;

where the attachment bus is a Universal Serial Bus (USB), and the first type of transfer associated with the first class of data is an isochronous transfer, and the second type of transfer associated with the second class of data is a bulk transfer.

Claim 7. (Previously Presented) The system of claim 3, where the peripheral device is configured to deliver the data in packets of predetermined length.

Claim 8. (Previously Presented) The system of claim 7, where the classifying circuit is configured to place each of the packets into one of the queues.

Claim 9. (Currently amended) A computer system comprising:

a host processor;

an attachment bus coupled to the host processor, the attachment bus being inside the computer system;

a peripheral device coupled to the host processor via the attachment bus, the peripheral device being configured to transfer data from a network to the host processor over ~~an~~ the attachment bus inside the computer system using at least first and second types of data transfers, comprising:

a classifying circuit configured to separate the data into a first class associated with the first type of

transfer and a second class associated with the second type of transfer;

a first queue connected to receive the first class of data from the classifying circuit;

a second queue connected to receive the second class of data from the classifying circuit; and

a control circuit configured to place data from the first queue onto the attachment bus at a higher priority than data from the second queue is placed onto the attachment bus;

where the attachment bus is configured to receive data during time cycles of predetermined length; where ~~a portion of~~ each packet ~~indicates~~ includes a virtual channel identifier ~~associated with the packet~~, and where the classifying circuit includes a storage device that stores ~~information indicating each of the~~ a list of virtual ~~channels~~ channel identifiers that are ~~is~~ associated with at least one of the classes.

Claim 10. (Currently amended) The system of claim 9, where the classifying circuit includes a selection element configured to (a) compare~~, for each packet, the information in the storage device to~~ the virtual channel identifier ~~data~~ in the ~~portion of the~~ packet ~~that indicates a virtual channel~~ to the virtual channel identifiers stored in the storage device and (b) select a corresponding one of the queues to receive the packet.

Claim 11-12 (Cancelled).

Claim 13. (Currently amended) A method comprising:

transferring data from a network to a host processor over an attachment bus inside the computer system using at least first and second types of data transfers and, in transferring the data:

separating the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer;

placing data of the first class onto the attachment bus at a higher priority than data of the second class is placed onto the attachment bus;

placing data on the attachment bus during time cycles of predetermined length, where placing data of the first class on the attachment bus includes placing at least a minimum amount of data of the first class onto the attachment bus during each time cycle; and

placing data of the second class onto the attachment bus only when the attachment bus is otherwise unoccupied by first class data.

Claim 14. (Previously Presented) The method of claim 13, further comprising receiving the data from a computer network.

Claim 15. (Previously Presented) The method of claim 13, where receiving the data includes receiving packetized voice data.

Claim 16. (Previously Presented) The method of claim 13, where transferring data includes delivering the data in packets of predetermined length.

Claim 17. (Previously Presented) The method of claim 16, where separating the data includes placing each of the packets into one of a plurality of queues.

Claim 18. (Currently amended) A method comprising:

transferring data from a network to a host processor over an attachment bus inside the computer system using at least first and second types of data transfers and, in transferring the data:

separating the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer;

placing data of the first class onto the attachment bus at a higher priority than data of the second class is placed onto the attachment bus;

placing data on the attachment bus during time cycles of predetermined length; and

storing ~~information indicating each~~ virtual channel identifiers that are ~~is~~ associated with at least one of the classes.

Claim 19. (Currently amended) The method of claim 18, further comprising:

comparing~~, for each packet, the stored information to~~ a ~~portion of the data~~ virtual circuit identifier in the packet ~~that indicates the virtual channel associated with the packet~~ to the stored virtual channel identifiers; and

responsive to said comparing, placing the packet into a corresponding one of the queues.

Claim 20. (Currently amended) The system of claim 9, where the classifying circuit comprises a buffer adapted to buffer a received packet, a shift register adapted to store a portion of the received packet, and the storage device is a content addressable memory (CAM) device adapted to store ~~information indicating each of the~~ virtual ~~channels~~ channel identifiers that ~~is~~ are associated with at least one of the classes.

Claim 21. (Currently amended) The system of claim 3, wherein the attachment bus is a Peripheral Component Interface (PCI) bus.

Claim 22. (Currently amended) The system of claim 3, wherein the ~~bus~~ network is ~~uses~~ an Asynchronous Transfer Mode (ATM) network.

Claim 23. (Currently amended) A peripheral device coupled between a host device and a network, the peripheral device operable to transfer data packets from the network to the host device ~~processor~~ over a bus inside the computer system, the peripheral device comprising:

a classifying circuit operable to identify a priority level of each data packet from the network;

a first queue operable to store data packets with a first priority level from the classifying circuit;

a second queue operable to store data packets with a second priority level from the classifying circuit; and

a control circuit coupled to first and second queues, the control circuit being operable to place data from the

first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

where the bus is configured to receive data during time cycles of predetermined length; the control circuit being configured to place at least a minimum amount of data from the first queue onto the bus during each time cycle; the control circuit being configured to place data from the second queue onto the bus only when the bus is otherwise unoccupied by first class data.

Claim 24. (Currently amended) A peripheral device coupled between a host device and a network, the peripheral device operable to transfer data packets from the network to the host device ~~processor~~ over a bus, the peripheral device comprising:

a classifying circuit operable to identify a priority level of each data packet from the network;

a first queue operable to store data packets with a first priority level from the classifying circuit;

a second queue operable to store data packets with a second priority level from the classifying circuit; and

a control circuit coupled to the first and second queues, the control circuit being operable to place data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

where the bus is a Universal Serial Bus (USB), and the first type of transfer associated with the first class is an isochronous transfer, and the second type of transfer associated with the second class is a bulk transfer.